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Abstract
Fuzzy logic controllers (FLCs), based on expert systems and rule-based approximate reasoning, have been successfully applied to control the dynamic, complex, and ill-defined systems. The key benefit of FLC is that the system behavior could be represented with simple “if-then” relations instead of complex mathematical models. By using the linguistic rules which capture the approximate and qualitative aspects of human knowledge, the FLC can infer desired output actions properly.

This thesis focused on the designs of three components: input fuzzifier, fuzzy inference unit, and defuzzifier. The input fuzzifier is used to generate proper membership functions correctly and quickly for FLC. Here, we presented two efficient VLSI architectures to generate the triangle-shaped and trapezoid-shaped membership functions, respectively. By inferring the active rules only, we designed an efficient fuzzy inference unit to implement the inference process in parallel and quickly. Finally, a new architecture is proposed to implement the defuzzifier. Compared with previous designs, our defuzzifier can implement the COG (Center of Gravity) defuzzification faster and more efficient.

The whole FLC architecture is synthesized with the standard-cell from TSMC’s cell library. The gate count of it is about 41000, and the chip size is 4247.5 um* 3544.2 um. It can yield an inference rate of 10M inferences/sec operating at a clock rate of 40MHz. The hardware architecture is also implemented with an Altera FLEX10K FPGA chip. A fuzzy temperature control system is built by integrating the chip with an 8051 microprocessor and the motor circuit to verify the performance of our FLC.
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